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Terms	Documents
L4 and (SOI or (silicon adj on adj insulator))	11

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EPO Abstracts Database	
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L8

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result set

*DB=DWPI; PLUR=YES; OP=ADJ*

L1 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

2 L1*DB=TDBD; PLUR=YES; OP=ADJ*

L2 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

2 L2*DB=USPT; PLUR=YES; OP=ADJ*

L3 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

484 L3*DB=PGPB; PLUR=YES; OP=ADJ*

L4 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

69 L4*DB=JPAB; PLUR=YES; OP=ADJ*

L5 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

0 L5*DB=EPAB; PLUR=YES; OP=ADJ*

L6 semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)

0 L6*DB=USPT; PLUR=YES; OP=ADJ*

L7 L3 and (SOI or (silicon adj on adj insulator))

100 L7*DB=PGPB; PLUR=YES; OP=ADJ*

L8 L4 and (SOI or (silicon adj on adj insulator))

11 L8

END OF SEARCH HISTORY

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**Search Results - Record(s) 1 through 2 of 2 returned.**☐ 1. Document ID: KR 2001053649 A

L1: Entry 1 of 2

File: DWPI

Jul 2, 2001

DERWENT-ACC-NO: 2002-047167

DERWENT-WEEK: 200206

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TITLE: Isolation method of semiconductor device

&lt; br&gt;Patent Assignee Terms:

HYNIX SEMICONDUCTOR INC

Patent Assignee Terms:

HYNIX SEMICONDUCTOR INC

Basic Abstract Text:

NOVELTY - An isolation method of a semiconductor memory device is provided to simplify a process by forming an auto-planarized isolation film, by using a deposition rate difference of an oxide between on a nitride film and on a silicon substrate around a trench by filling the trench with the oxide formed an APCVD.

Basic Abstract Text:

DETAILED DESCRIPTION - A buffer oxide(21) is formed on a silicon substrate(20) by a thermal oxidation method, and a mask layer(22) is formed by depositing a silicon nitride on the buffer oxide by a CVD(Chemical Vapor Deposition) method. And, an etch mask(22) confining an isolation region and an active region is formed by patterning the mask layer and the buffer oxide. Then, a trench is formed by etching a revealed isolation region using a RIE(Reactive Ion Etching) or a plasma etching method. A high temperature thermal oxide is grown on the surface of the silicon substrate revealed by the formation of the trench. And, the surface of the silicon substrate is revealed again by wet-etching the high temperature thermal oxide to cure a defective part of the substrate. An insulation film(240) is deposited on the etch mask enough thick to fill the revealed trench using an APCVD(Atmospheric Pressure Chemical Vapor Deposition) method. Then, the surface of the etch mask is revealed by performing a CMP(chemical mechanical polishing) to planarize the insulation film where an isolation film is to be formed.

Standard Title Terms:

ISOLATE METHOD SEMICONDUCTOR DEVICE

Patent Assignee Terms (1):

HYNIX SEMICONDUCTOR INC

Patent Assignee Terms (1):

HYNIX SEMICONDUCTOR INC

Title (1):

Isolation method of semiconductor device

Basic Abstract Text (1):

NOVELTY - An isolation method of a semiconductor memory device is provided to simplify a process by forming an auto-planarized isolation film, by using a deposition rate difference of an oxide between on a nitride film and on a silicon substrate around a trench by filling the trench with the oxide formed an APCVD.

Basic Abstract Text (2):

DETAILED DESCRIPTION - A buffer oxide(21) is formed on a silicon substrate(20) by a thermal oxidation method, and a mask layer(22) is formed by depositing a silicon nitride on the buffer oxide by a CVD(Chemical Vapor Deposition) method. And, an etch mask(22) confining an isolation region and an active region is formed by patterning the mask layer and the buffer oxide. Then, a trench is formed by etching a revealed isolation region using a RIE(Reactive Ion Etching) or a plasma etching method. A high temperature thermal oxide is grown on the surface of the silicon substrate revealed by the formation of the trench. And, the surface of the silicon substrate is revealed again by wet-etching the high temperature thermal oxide to cure a defective part of the substrate. An insulation film(240) is deposited on the etch mask enough thick to fill the revealed trench using an APCVD(Atmospheric Pressure Chemical Vapor Deposition) method. Then, the surface of the etch mask is revealed by performing a CMP(chemical mechanical polishing) to planarize the insulation film where an isolation film is to be formed.

Standard Title Terms (1):

ISOLATE METHOD SEMICONDUCTOR DEVICE

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 2. Document ID: US 5741740 A

L1: Entry 2 of 2

File: DWPI

Apr 21, 1998

DERWENT-ACC-NO: 1998-260520

DERWENT-WEEK: 199824

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TITLE: Forming a shallow trench isolation with a gap-filling silicon oxide trench-fill layer - by a sub-atmospheric pressure thermal chemical vapour deposition method using ozone and a tetra-ethyl orthosilicate as the silicon source material

Patent Assignee Terms:

TAIWAN SEMICONDUCTOR MFG CO LTD

Patent Assignee Terms:

TAIWAN SEMICONDUCTOR MFG CO LTD

Basic Abstract Text:

A method is claimed for filling a trench within a silicon substrate comprising the steps: (a) thermally oxidising the Si substrate having a trench therein so as to form an oxide liner to the trench; (b) forming a conformal Si oxide intermediate layer upon the thermal oxide liner, using plasma-enhanced chemical vapour deposition (PECVD) with silane as the Si source; and (c) forming upon the conformal Si oxide intermediate layer a gap-filling Si oxide trench-fill layer by a sub-atmospheric pressure thermal CVD method using ozone and a tetra-ethyl orthosilicate as the Si source material.

Basic Abstract Text:

Also claimed is a silicon substrate having a trench therein which is filled by a gap-filling silicon oxide trench-fill layer as above.

Basic Abstract Text:

ADVANTAGE - The bulk quality of the Si oxide trench-fill layer is improved, as demonstrated by its etch rate in dilute HF. The Si oxide trench-fill layer has a reduced surface roughness, and is less sensitive to the surface on which it is formed.

Standard Title Terms:

FORMING SHALLOW TRENCH ISOLATE GAP FILL SILICON OXIDE TRENCH FILL LAYER SUB ATMOSPHERE PRESSURE THERMAL CHEMICAL VAPOUR DEPOSIT METHOD OZONE TETRA ETHYL ORTHOSILICATE SILICON SOURCE MATERIAL

Patent Assignee Terms (1):

TAIWAN SEMICONDUCTOR MFG CO LTD

Patent Assignee Terms (1):

TAIWAN SEMICONDUCTOR MFG CO LTD

Title (1):

Forming a shallow trench isolation with a gap-filling silicon oxide trench-fill layer - by a sub-atmospheric pressure thermal chemical vapour deposition method using ozone and a tetra-ethyl orthosilicate as the silicon source material

Basic Abstract Text (1):

A method is claimed for filling a trench within a silicon substrate comprising the steps: (a) thermally oxidising the Si substrate having a trench therein so as to form an oxide liner to the trench; (b) forming a conformal Si oxide intermediate layer upon the thermal oxide liner, using plasma-enhanced chemical vapour deposition (PECVD) with silane as the Si source; and (c) forming upon the conformal Si oxide intermediate layer a gap-filling Si oxide trench-fill layer by a sub-atmospheric pressure thermal CVD method using ozone and a tetra-ethyl orthosilicate as the Si source material.

Basic Abstract Text (2):

Also claimed is a silicon substrate having a trench therein which is filled by a gap-filling silicon oxide trench-fill layer as above.

Basic Abstract Text (4):

ADVANTAGE - The bulk quality of the Si oxide trench-fill layer is improved, as demonstrated by its etch rate in dilute HF. The Si oxide trench-fill layer has a reduced surface roughness, and is less sensitive to the surface on which it is formed.

Standard Title Terms (1):

FORMING SHALLOW TRENCH ISOLATE GAP FILL SILICON OXIDE TRENCH FILL LAYER SUB ATMOSPHERE PRESSURE THERMAL CHEMICAL VAPOUR DEPOSIT METHOD OZONE TETRA ETHYL ORTHOSILICATE SILICON SOURCE MATERIAL

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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Terms	Documents
semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)	2

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: NN8804448

L2: Entry 1 of 2

File: TDBD

Apr 1, 1988

TDB-ACC-NO: NN8804448

DISCLOSURE TITLE: Polish Stop Structure for Oxide-Filled Semiconductor Trenches

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, April 1988, US

VOLUME NUMBER: 30

ISSUE NUMBER: 11

PAGE NUMBER: 448 - 449

PUBLICATION-DATE: April 1, 1988 (19880401)

CROSS REFERENCE: 0018-8689-30-11-448

DISCLOSURE TEXT:

- A process is disclosed for using a refractory metal and/or refractory silicide as a planarization polish stop for polishing oxide materials used to fill shallow isolation trenches fabricated in the CMOS technology. Silicon dioxide is the obvious choice of insulators to use for filling shallow isolation trenches. Unfortunately, polishing processes do not work well for structures wherein the polish step is intended to remove oxide, due to a poor polish rate ratio between oxide and nitride (etch stop). This leads to cross-wafer uniformity problems, difficulties in removing oxide over large untrenched regions, and end point detection problems. The following structure requirements should be considered when replacing nitride as the polish stopping film for oxide filled trenches: 1) A proper reactive ion etch (RIE) mask material should be provided on top of the structure when forming trenches. The mask material of choice for most RIE trenching processes is silicon dioxide. 2) Because thermal oxide is grown on the side walls of newly formed trenches to remove any RIE damage to the silicon, the RIE mask material should protect active device regions from oxidation during thermal oxide growth. 3) The mask material should not be attacked by acids used to remove sacrificial silicon dioxide films on trench sidewalls. 4) The mask should polish slowly relative to the trench fill. 5) Mask stripping must not damage the underlying active regions or the trench fill. A new masking structure is shown in Fig. 1 composed of a thin thermal oxide pad 10 on a silicon substrate 11, a refractory metal or a refractory metal silicide 12, in combination with a polysilicon layer 13 to enhance oxidation, and a silicon dioxide capping layer 14. The refractory metal or silicide 12 is employed as a polish resistant layer (etch stop) to protect the underlying single crystal regions from oxidation during trench sidewall passivation. A silicon dioxide cap 14 is employed as a mask for the shallow isolation trench RIE. To form the stack structure shown in Fig. 1, a thermal oxide pad 10-25nm thick is formed on top of the silicon substrate. A refractory metal silicide film with a polysilicon layer (polycide) may be chosen over a refractory metal because polycides behave well under most oxidation conditions. The thickness of the refractory layer is determined by the relative polish rates of it to the oxide fill used in the shallow isolation trench. A chemical vapor deposition (CVD) of silicon dioxide forms a cap approximately 300 nm thick on top of the structure is utilized as a RIE mask. The isolation trench pattern is defined using conventional photolithographic techniques. Fig. 2 shows the structure after a RIE through the oxide/refractory/oxide stack 15 is performed and the resist is stripped. Fig. 3 shows

the trench 16 formed by a RIE. The trench sidewalls are passivated with a thermal oxide 17. Optionally, nitride 18 may be deposited as a further sidewall passivation layer. The trench is filled (not shown) with CVD silicon dioxide or nitride. The fill material is then polished, stopping on the refractory metal. Finally, the refractory layer and the underlying pad are removed using conventional methods. At this point the structure is ready for the formation of active devices.

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KVMC

## 2. Document ID: NN86034547

L2: Entry 2 of 2

File: TDBD

Mar 1, 1986

TDB-ACC-NO: NN86034547

DISCLOSURE TITLE: Partial Polycrystalline Silicon-Filled Trench for VLSI

## PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, March 1986, US

VOLUME NUMBER: 28

ISSUE NUMBER: 10

PAGE NUMBER: 4547 - 4550

PUBLICATION-DATE: March 1, 1986 (19860301)

CROSS REFERENCE: 0018-8689-28-10-4547

## DISCLOSURE TEXT:

- Over-planarization may occur in polycrystalline silicon-filled trench (PST) isolation processes for VLSI (very large-scale integration) in semiconductor devices. This recesses the fill below the wafer surface and may expose epitaxy regions causing electrical shorts. In addition to N-epi shorting to the substrate, stress can result from oxidizing the filled poly-Si through poly-Si voids in the deep trench region. This article proposes a process for protecting the poly at appropriate steps so as to overcome these problems. Fig. 1 shows the various films on N-type epi 8 grown on p-type silicon substrate 3 by means of a standard PST (poly-silicon trench) process. The other layers are N+ 9, LPCVD (low pressure chemical vapor deposition) oxide 4, Si<sub>3</sub>N<sub>4</sub> 5, thermal oxide 6 and ROI (recessed oxide isolation) 7. A multilayer resist (MLR) structure for deep trench image definition is on top of the LPCVD oxide and consists of two PR (photoresist) layers 1 and an LTO (low temperature oxide) layer 2. In the next step the deep trench 11 (Fig. 2) is formed by RIE (Reactive Ion etch) of the oxide-Si<sub>3</sub>N<sub>4</sub>-oxide sandwich with CHF<sub>3</sub> followed by a PR strip and then an RIE of the Si with CCl<sub>2</sub>F<sub>2</sub> + N<sub>2</sub>. The LPCVD oxide may have been etched down to 0.5 mm. Low temperature poly-Si 10 about 0.4 mm thick is then deposited and doped in situ. A thin layer of CVD (chemical vapor deposition) nitride (about 500 Angstroms) 5 is deposited. The remaining deep trench is filled with LPCVD oxide (1 mm) 4. A layer of 1.5 mm thick PR 1 is applied, and the wafer is ready for planarization. The structure after planarization is shown in Fig. 3. This is achieved by first an RIE of the PR 1 and SiO<sub>2</sub> 4 (Fig. 2) in CF<sub>4</sub> followed by an RIE of the SiO<sub>2</sub> in CCl<sub>2</sub>F<sub>3</sub> + H<sub>2</sub> they\*U which has the etch ratio of SiO<sub>2</sub> : Si about 70:1, and SiO<sub>2</sub> : Si<sub>3</sub>N<sub>4</sub> about 10:1. After planarization, about 300 Angstroms of Si<sub>3</sub>N<sub>4</sub> 5 is left (Fig. 3). LPCVD oxide 4 is deposited for poly-Si definition masking. Unwanted poly-Si is then etched away in CCl<sub>2</sub>F<sub>2</sub> + O<sub>2</sub>. After the masking, SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> is etched out in CHF<sub>3</sub>. After poly-Si definition, CVD oxide 4 (Fig.

4) is deposited for substrate contact masking. The contact hole is defined and etched out in CHF3, followed by metallization 14, and the final structure is as shown in Fig. 4. The new trench structure offers the following advantages: 1. The poly-Si layer serves as an etch stop due to high rate differential between SiO2 and Si. Adverse effects due to overplanarization, such as an N-epi short to substrate, can be avoided. 2. The poly-Si provides substrate contact of any geometry with low contact resistance. 3. The poly-Si can act as a cushion to relieve stress due to oxidation. 4. It can be applied to non-ROI schemes. Reference they\*Ü R. S. Bennett, "Highly Selective Etching of SiO2 Using CClF3 H2," IBM Technical Disclosure Bulletin 25, 4589 (February 1983).

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semiconductor and substrate and (trench or groove) and (thermal adj oxide) and ((silicon or polysilicon) near4 fill\$) and (vapor adj deposition)	2

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☐ 1. Document ID: US 20020022326 A1

L8: Entry 1 of 11

File: PGPB

Feb 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020022326

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020022326 A1

TITLE: Semiconductor device and method of manufacturing the same

PUBLICATION-DATE: February 21, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kunikiyo, Tatsuya	Tokyo		JP	

US-CL-CURRENT: 438/296

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWC

☐ 2. Document ID: US 20020022308 A1

L8: Entry 2 of 11

File: PGPB

Feb 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020022308

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020022308 A1

TITLE: Method of preventing semiconductor layers from bending and semiconductor device formed thereby

PUBLICATION-DATE: February 21, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ahn, Dong-Ho	Yongin-shi		KR	
Kang, Ho-Kyu	Yongin-shi		KR	
Bae, Geum-Jong	Yongin-shi		KR	

US-CL-CURRENT: 438/164; 257/347, 438/219, 438/296, 438/318

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWC

☐ 3. Document ID: US 20020017133 A1

L8: Entry 3 of 11

File: PGPB

Feb 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020017133  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020017133 A1

TITLE: Surface/bulk micromachined single-crystalline silicon micro-gyroscope

PUBLICATION-DATE: February 14, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Cho, Dong-il	Seoul		KR	

US-CL-CURRENT: 73/504.02; 73/504.08, 73/504.18

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 4. Document ID: US 20020014673 A1

L8: Entry 4 of 11

File: PGPB

Feb 7, 2002

PGPUB-DOCUMENT-NUMBER: 20020014673  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020014673 A1

TITLE: Method of making membrane integrated circuits

PUBLICATION-DATE: February 7, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Leedy, Glenn Joseph	Montecito	CA	US	

US-CL-CURRENT: 257/419; 257/415, 257/417, 257/619, 438/459, 438/50, 438/51, 438/53

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 5. Document ID: US 20020009874 A1

L8: Entry 5 of 11

File: PGPB

Jan 24, 2002

PGPUB-DOCUMENT-NUMBER: 20020009874  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020009874 A1

TITLE: Buried conductors

PUBLICATION-DATE: January 24, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Farrar, Paul A.	So. Burlington	VT	US	
Noble, Wendell P.	Milton	VT	US	

US-CL-CURRENT: 438/620

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

KWIC

☐ 6. Document ID: US 20020001871 A1

L8: Entry 6 of 11

File: PGPB

Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020001871  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020001871 A1

TITLE: Triple layer isolation for silicon microstructure and structures formed using the same

PUBLICATION-DATE: January 3, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Cho, Dong-Il	Seoul		KR	
Lee, Sangwoo	Seoul		KR	
Park, Sangjun	Seoul		KR	

US-CL-CURRENT: 438/98; 438/411

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

KWIC

☐ 7. Document ID: US 20010044188 A1

L8: Entry 7 of 11

File: PGPB

Nov 22, 2001

PGPUB-DOCUMENT-NUMBER: 20010044188  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010044188 A1

TITLE: Method of fabricating memory cell

PUBLICATION-DATE: November 22, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Heo, Kuen-Chy	Chiai Hsien		TW	
Lin, Jeng-Ping	Taoyuan Hsien		TW	

US-CL-CURRENT: 438/268; 438/241, 438/243, 438/270

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

KWIC

☐ 8. Document ID: US 20010042871 A1

L8: Entry 8 of 11

File: PGPB

Nov 22, 2001

PGPUB-DOCUMENT-NUMBER: 20010042871  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010042871 A1

TITLE: SILICON-ON-INSULATOR ISLANDS

PUBLICATION-DATE: November 22, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
NOBLE, WENDELL P	MILTON	VT	US	

US-CL-CURRENT: 257/254; 257/508

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 9. Document ID: US 20010031514 A1

L8: Entry 9 of 11

File: PGPB

Oct 18, 2001

PGPUB-DOCUMENT-NUMBER: 20010031514  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010031514 A1

TITLE: Method and apparatus for fabricating self-assembling microstructures

PUBLICATION-DATE: October 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, John Stephen	Berkeley	CA	US	

US-CL-CURRENT: 438/107; 257/13, 257/94, 257/98, 438/113, 438/28

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 10. Document ID: US 20010023094 A1

L8: Entry 10 of 11

File: PGPB

Sep 20, 2001

PGPUB-DOCUMENT-NUMBER: 20010023094  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010023094 A1

TITLE: Method for manufacturing a SOI wafer

PUBLICATION-DATE: September 20, 2001

INVENTOR-INFORMATION:

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Search Results - Record(s) 11 through 11 of 11 returned.

☐ 11. Document ID: US 20010013630 A1

L8: Entry 11 of 11

File: PGPB

Aug 16, 2001

PGPUB-DOCUMENT-NUMBER: 20010013630

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010013630 A1

TITLE: Isolation in micromachined single crystal silicon using deep trench insulation

PUBLICATION-DATE: August 16, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Cho, Dong-Il	Seoul		KR	
Lee, Sangwoo	Seoul		KR	
Park, Sangjun	Seoul		KR	
Lee, Sangchul	Seoul		KR	

US-CL-CURRENT: 257/419; 438/53

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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Terms	Documents
L4 and (SOI or (silicon adj on adj insulator))	11

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File: PGPB

Aug 16, 2001

PGPUB-DOCUMENT-NUMBER: 20010013630

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010013630 A1

TITLE: Isolation in micromachined single crystal silicon using deep trench insulation

PUBLICATION-DATE: August 16, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Cho, Dong-Il	Seoul		KR	
Lee, Sangwoo	Seoul		KR	
Park, Sangjun	Seoul		KR	
Lee, Sangchul	Seoul		KR	

US-CL-CURRENT: 257/419; 438/53

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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Terms	Documents
L4 and (SOI or (silicon adj on adj insulator))	11

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1	CTNF	4
2	892	1
3	1449	1

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